iW-RainboW-G23S
RZ/G1C Single Board Computer
Hardware User Guide

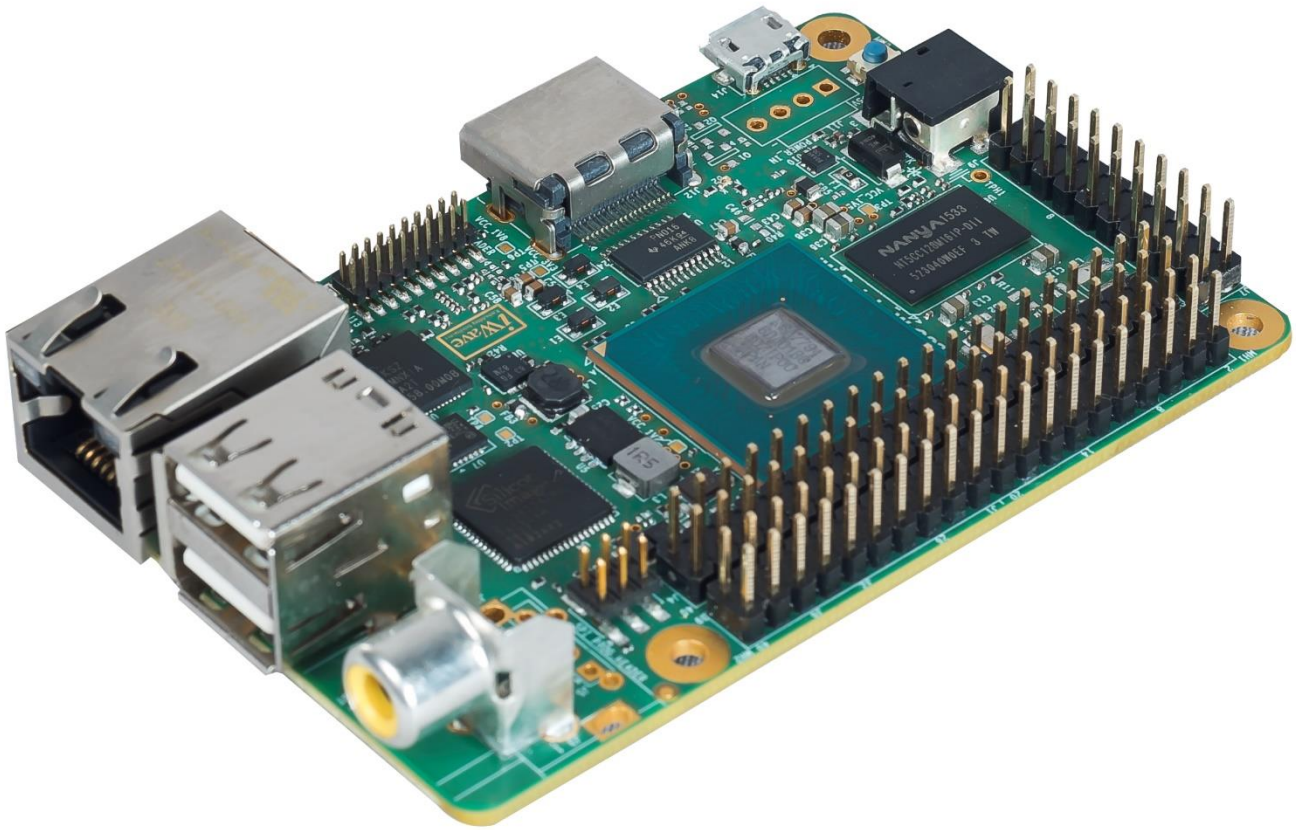

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Table of Contents

List of Figures

List of Tables

1. INTRODUCTION

1.1 Purpose

This document is the Hardware User Guide for the RZ/G1C SBC based on the Renesas's RZ/G1C Application processor. This board is fully supported by iWave Systems Technologies Pvt. Ltd. This Guide provides detailed information on the overall design and usage of the RZ/G1C SBC from a Hardware Systems perspective.

1.2 Renesas SBC Overview

The RZ/G1C Single Board Computer is an extension of RZ/G1C CPU. Also with the SBC approach that integrates all the core components of a common PC. RZ/G1C SBC has a form factor of 85mm x 56mm and provides the functional requirements for an embedded application.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
ARM	Advanced RISC Machine
BPP	Bits Per Pixel
BSP	Board Support Package
CAN	Controller Area Network
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
CVBS	Composite Video Baseband Signal
DDR3	Double Data Rate 3
eMMC	Enhanced Multi Media Card
GB	Giga Byte
Gbps	Gigabits per sec
GPIO	General Purpose Input Output
HSCIF	High Speed Serial Communication Interface with FIFO
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
JTAG	Joint Test Action Group
Kbps	Kilobits per second
LVDS	Low Voltage Differential Signalling
MAC	Media Access Controller
MB	Mega Byte
Mbps	Megabits per sec
MHz	Mega Hertz

Acronyms	Abbreviations
MMCIF	Multi-media card interface
MSIOF	Clock-Synchronized Serial Interface with FIFO
NPTH	Non Plated Through hole
PCB	Printed Circuit Board
PTH	Plated Through hole
PWM	Pulse Width Modulation
QSPI	Quad Serial Peripheral Interface
SBC	Single Board Computer
SCIF	Serial Communication Interface with FIFO
SD	Secure Digital
SDHI	SD Card Host Interface
SSI	Serial Sound Interface
SDRAM	Synchronous Dynamic Random Access Memory
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
USB OTG	USB On The Go

1.4 Terminlogy Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
DIFF	Differential Signal
LVDS	Low Voltage Differential Signal
OD	Open Drain Signal
OC	Open Collector Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented On-SBC.

1.5 References

- RZ/G1C CPU Hardware User Manual

1.6 Important Note

RZ/G1C SBC signal name is followed as per below format for easy understanding.

- If CPU pin has multiplexing option and selected particular function, then the signal name is mentioned as

  "Selected Function Name (GPIO Number)"

  Example: CAN0_RX(GP6_14)

  In this signal, ***CAN0_RX*** is the functionality which we are using and ***GP6_14*** is the GPIO number.

- If CPU pin has multiplexing option and selected as GPIO function, then the signal name is mentioned as

  "GPIO (GPIO Number)"

  Example: GPIO(GP4_1)

  In this signal, ***GPIO*** is MUX functionality which we are using and ***GP4_1*** is the GPIO number.

- If CPU pin doesn't have multiplexing option, then the signal name is mentioned as,

  "Function name"

  Example: USB0_DP

  In this signal, functionality which we are using is ***USB0_DP***

Note: The above naming is not applicable for other signals which are not connected to CPU.

2. ARCHITECTURE AND DESIGN

This section provides detailed information about the RZ/G1C SBC features and Hardware architecture with high level block diagram. Also, this section provides detailed information about SBC Expansion connectors pin assignment and usage.

2.1 RZ/G1C SBC Block Diagram

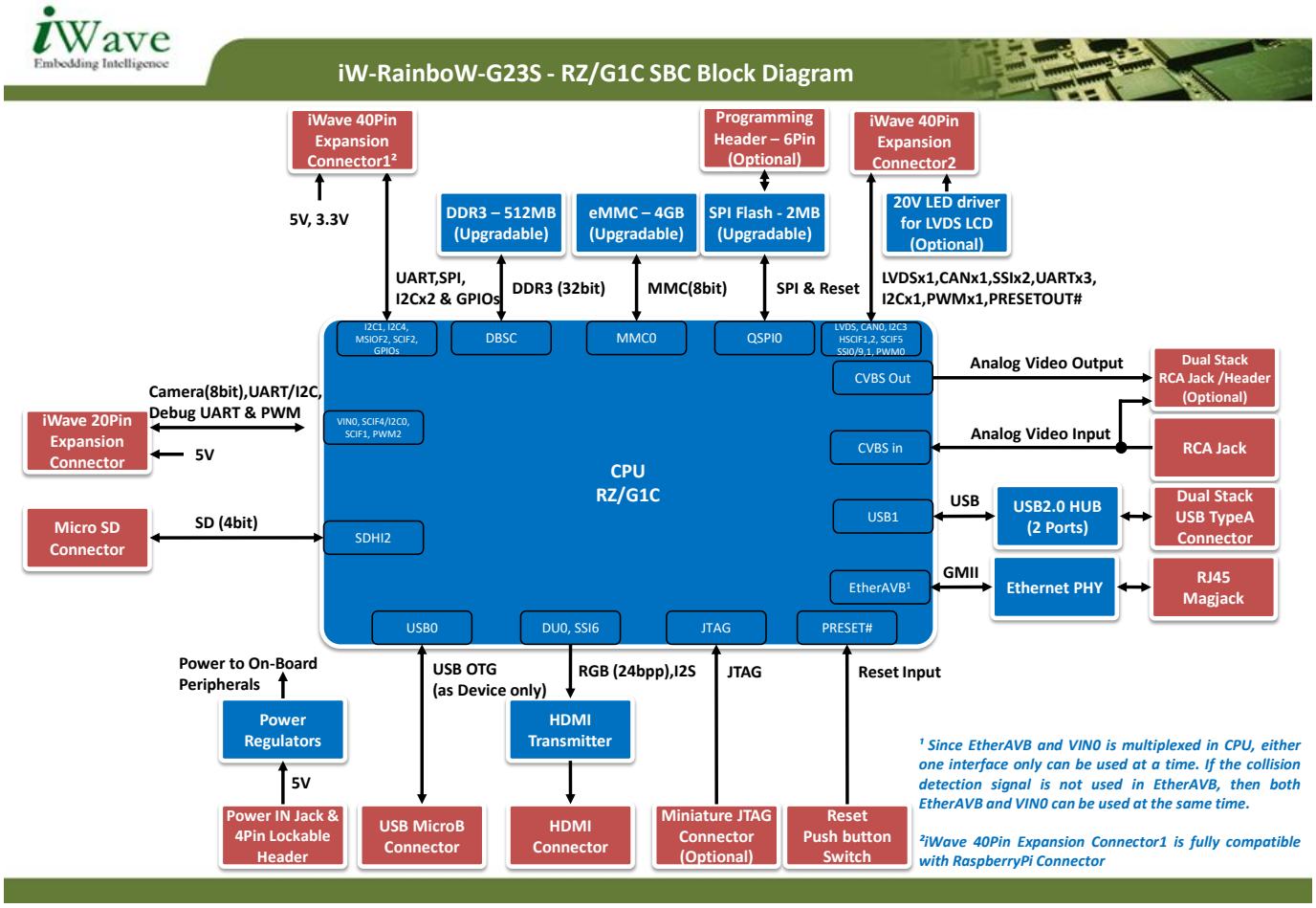

Figure 1: RZ/G1C SBC Block Diagram

2.2 RZ/G1C SBC Features

The RZ/G1C Single Board computer supports the following features.

CPU

- Renesas' RZ/G1C Dual ARM Cortex®-A7 MPCore® @ 1GHz

Memory

- DDR3 SDRAM – 512 MB (Expandable)
- SPI Flash - 2MB (Expandable)
- eMMC Flash - 4GB (Expandable)
- Micro SD slot

Communication Features

- 100/1000Mbps Ethernet through RJ45 MagJack
- USB2.0 Host x 2 Ports through Dual Stack TypeA Connector
- USB2.0 OTG as Device x 1 Port through MicroB Connector

Video Features

- HDMI x 1 Port through HDMI connector
- Analog Video Input through RCA Jack

40 Pin Expansion Connector1 Interfaces

- SPI
- I2C x 2
- GPIO's
- Data UART (without CTS & RTS)
- PWM

40 Pin Expansion Connector2 Interfaces

- LVDS x 1
- CAN x 1
- SSI x 2
- DATA UART x 2 (with CTS & RTS)
- DATA UART x 1 (without CTS & RTS)
- I2C x 1
- PWM x 1

20 Pin Expansion Connector Interfaces

- Parallel Camera (VIN0 – 8bit) x 1 Port
- Debug UART
- Data UART (without CTS & RTS)/I2C
- PWM x 1

Other Features

- JTAG Header
- Reset Switch

General Specification

- Power Supply : 5V,2.5A
- Form Factor : 85mm x 56mm

2.3 RZ/G1C CPU

The RZ/G1C SBC is based on Renesas's RZ/G1C CPU with built-in Dual ARM Cortex®-A7 MPCore® which can operate up to 1 GHz/core. The Block Diagram of RZ/G1C CPU from Renesas's website is shown below for reference.

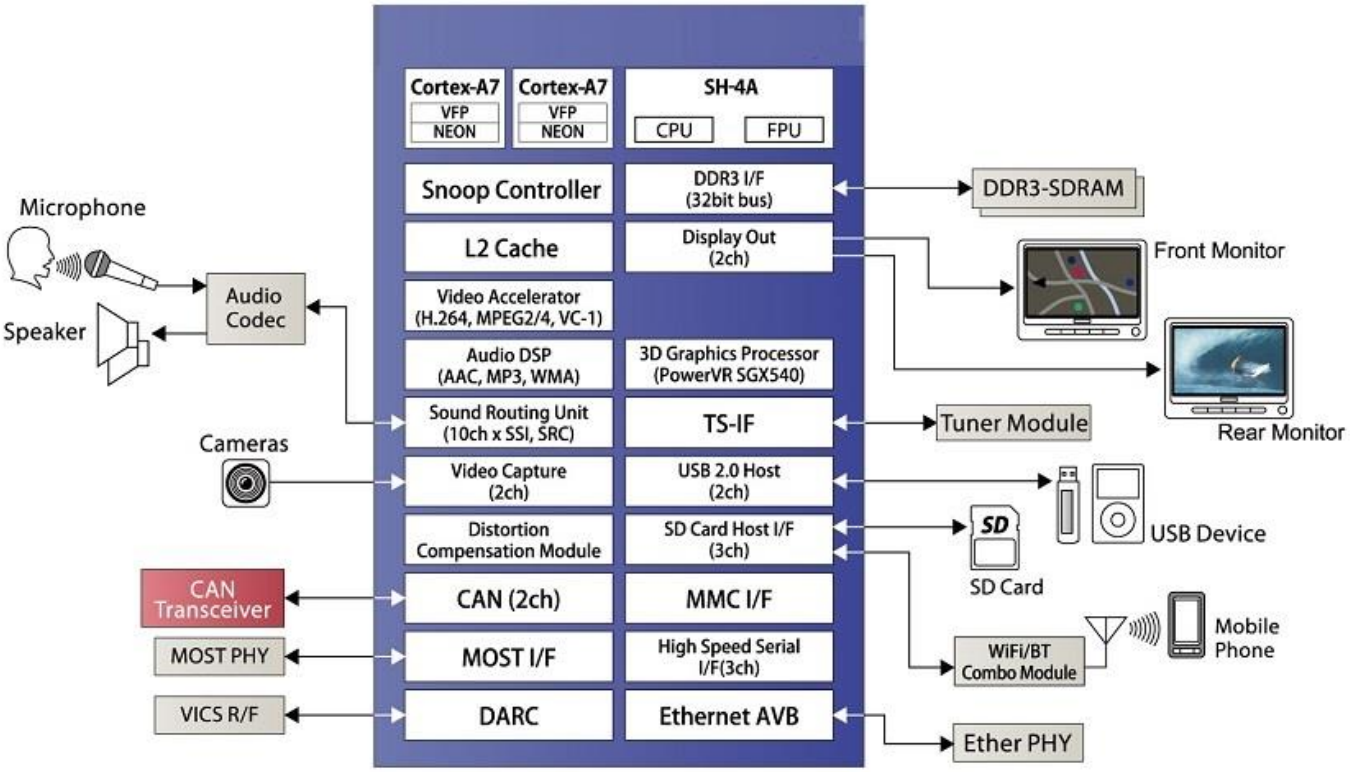

Figure 2: RZ/G1C Simplified Block Diagram

Note: Please refer the latest RZ/G1C Datasheet & Reference Manual for more details which may be revised from time to time.

2.4 Memory

2.4.1 DDR3 SDRAM

The RZ/G1C SBC supports 512MB DDR3 RAM memory by default. This is connected to CPU in 32bit x 1ch mode where it uses two 256MB DDR3-SDRAM ICs. This device operates at 1.5V voltage level. DDR3-SDRAM ICs are physically located on either side of the SBC. The RAM size can be expandable up to maximum of 2GB.

2.4.2 SPI NOR Flash

The RZ/G1C SBC supports 2MB SPI NOR Flash as default boot device. This is connected to QSPI controller of the RZ/G1C CPU and operates at 3.3 Voltage level. The SPI flash memory is physically located on bottom side of the SBC.

To program the boot code in to the SPI flash for the first time, use JTAG debugger through JTAG Header (J13) Optionally the external SPI programmer with 8pin SOIC test clips (Example part: 923655-08 from 3M). (or) through SPI Programming Header (J6) can be used for programming the SPI flash.

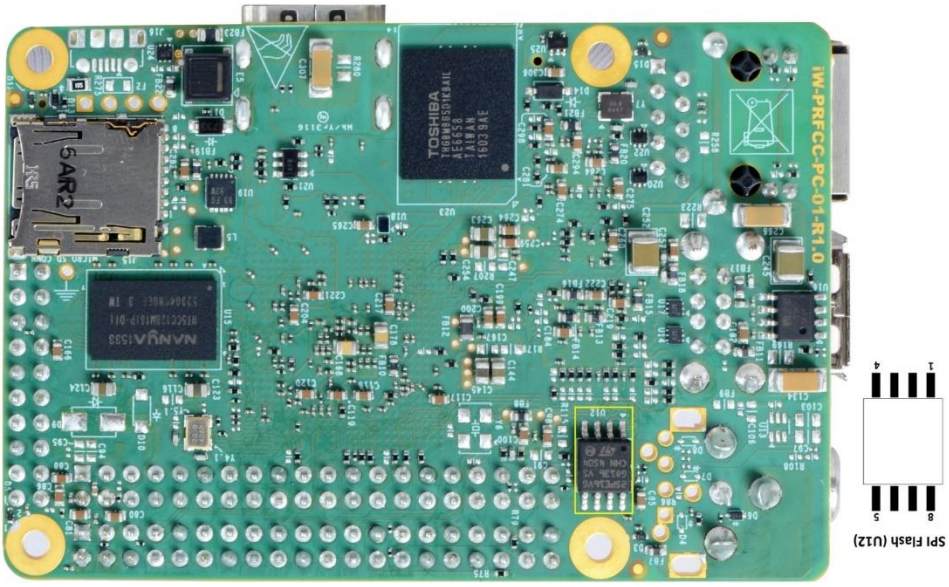

Figure 3: SPI Flash

2.4.3 eMMC Flash

The RZ/G1C SBC supports 4GB eMMC Flash memory as mass storage. eMMC is directly connected to the MMC0 controller of the RZ/G1C CPU which supports MMC 4.41 and operating at 3.3V Voltage level. The eMMC flash memory is physically located on bottom side of the SBC. The memory size of the eMMC Flash can be expandable.

2.4.4 Micro SD Slot

The RZ/G1C SBC supports Micro SD slot which can be used to connect Micro SD card as Mass storage. Micro SD card connector (J15) is directly connected to the SDHI2 controller of the RZ/G1C CPU. It also supports card detect feature through RZ/G1C GPIO “GP4_20”. The main power to Micro SD Card Connector is 3.3 Voltage. Micro SD Connector is physically located on bottom side of the SBC as shown below.

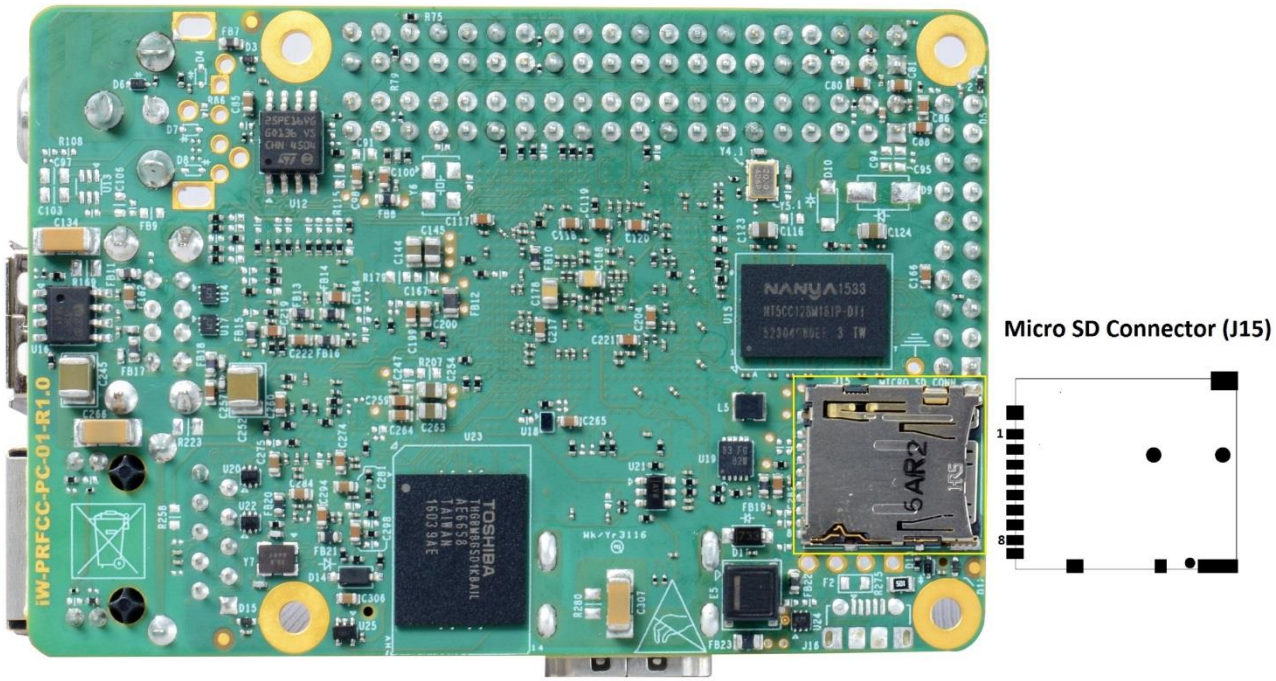

Figure 4: Micro SD Connector

2.5 Communication Features

2.5.1 100/1000Mbps Ethernet

The RZ/G1C SBC supports one 100/1000 Mbps Ethernet interface. The MAC is integrated in the RZ/G1C CPU and connected to the external Gigabit Ethernet PHY "KSZ9031MNX". RZ/G1C SBC also supports Link and Activity indication LED control signals.

The Gigabit Ethernet Connector is physically located on top side of the SBC.

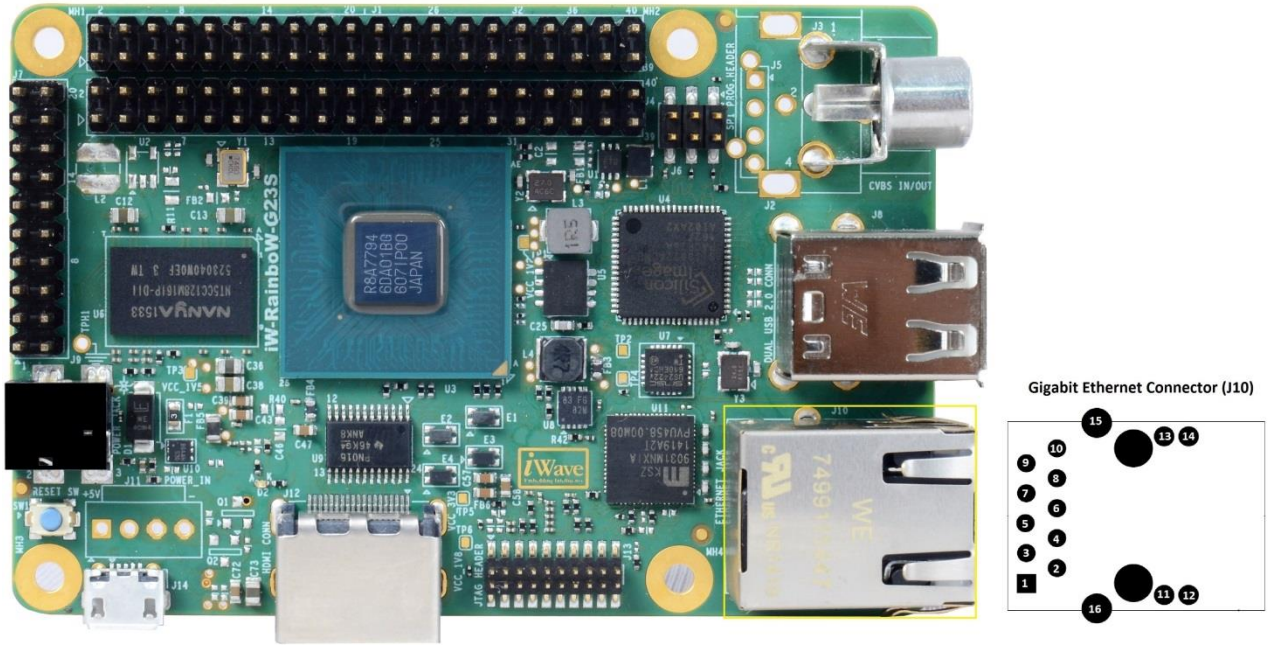

Figure 5: Gigabit Ethernet Connector

Table 3: RJ45 MagJack Pin Out

Pin No.	Pin Name	Signal Name	Signal Type/ Termination	Description
1	TRD1+	GPHY_ATXRXP	IO, DIFF	Gigabit Ethernet differential pair 1 positive.
2	TRD1-	GPHY_ATXRXM	IO, DIFF	Gigabit Ethernet differential pair 1 negative.
3	TRD2+	GPHY_BTXRXP	IO, DIFF	Gigabit Ethernet differential pair 2 positive
4	TRD2-	GPHY_BTXRXM	IO, DIFF	Gigabit Ethernet differential pair 2 negative.
5	TRCT1	TRCT_1	-	Transformer Centre Tap 1.
6	TRCT2	TRCT_2	-	Transformer Centre Tap 2.
7	TRD3+	GPHY_CTXRXP	IO, DIFF	Gigabit Ethernet differential pair 3 positive

Pin No.	Pin Name	Signal Name	Signal Type/ Termination	Description
8	TRD3-	GPHY_CTXRXM	IO, DIFF	Gigabit Ethernet differential pair 3 negative.
9	TRD4+	GPHY_DTXRXP	IO, DIFF	Gigabit Ethernet differential pair 4 positive
10	TRD4-	GPHY_DTXRXM	IO, DIFF	Gigabit Ethernet differential pair 4 negative.
11	Y-/G+	ETH1_LED-Y_K	I, 3.3V CMOS	Ethernet1 Speed indication Yellow LED Cathode.
12	Y+/G-	ETH1_LED-Y_A	I, 3.3V Power	Ethernet1 Speed indication Yellow LED Anode.
13	G+/Y	ETH1_LED-GO_A	I, 3.3V Power	Ethernet1 Link/Activity indication Green LED Anode.
14	G-/Y+	ETH1_LED-GO_K	I, 3.3V CMOS	Ethernet1 Link/Activity indication Green LED Anode.
15	MH1	ETH1_GND	Power	Ground
16	MH1	ETH1_GND	Power	Ground

2.5.2 USB 2.0 Host Interface

The RZ/G1C SBC supports one USB2.0 Host interface. RZ/G1C CPU's USB1 Host controller with integrated PHY is used USB Host interface which supports USB2.0 High-Speed (480 Mbps)/Full-Speed (12 Mbps)/Low-Speed (1.5 Mbps) transfer.

The RZ/G1C CPU's USB1 PHY output is connected to 2port USB HUB" USB2422-I/MJ". Two USB Ouput 1 & 2 from USB Hub is connected to USB Type A Dual stack connector (J8) . Also, over current input of USB Port1 is connected to RZ/G1C CPU's USB1_OVC(GP0_3) pins for over current detection. RZ/G1C CPU's USB1_PWEN(GP0_2) is connected to USB power switch to controlling USB1 & 2 VBUS power. The Dual Stack Connector is physically located on top side of the SBC.

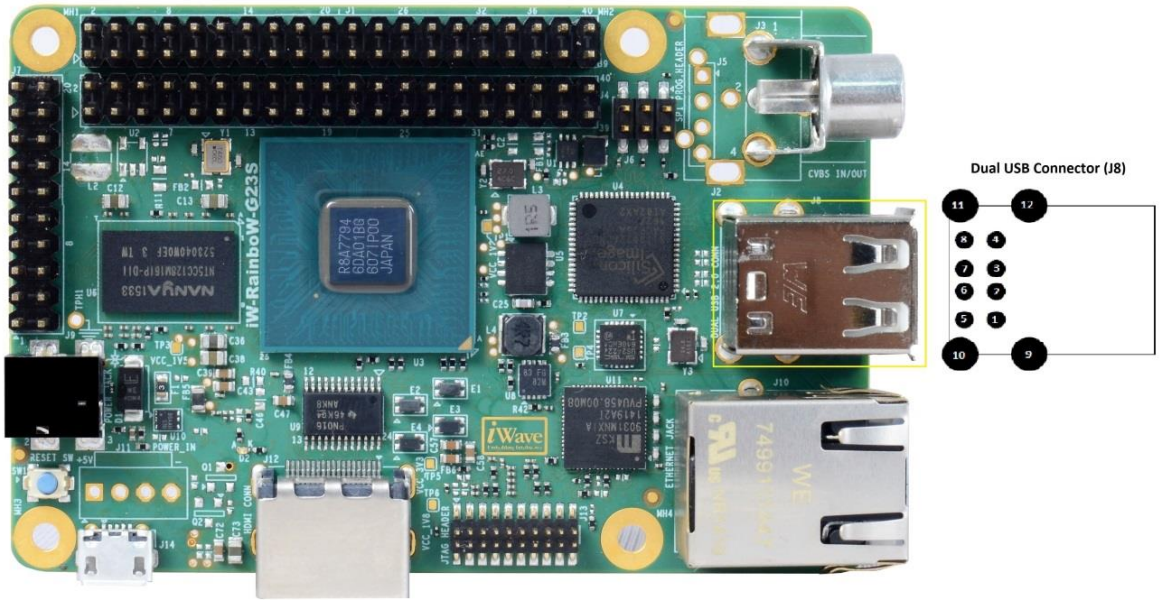

Figure 6: Dual USB Connector

Table 4: USB 2.0 Host Connector Pin Out

Pin No.	Pin Name	Signal Name	Signal Type/ Termination	Description
1	5V1	VBUS_HOST1	Power	5V Supply Voltage
2	D1-	USB_HUBP1_ DM	IO, DIFF	USB1 Host Data negative.
3	D1+	USB_HUBP1_DP	IO, DIFF	USB1 Host Data positive
4	GND	USB_GND	Power	Ground
5	5V2	VBUS_HOST2	Power	Ground
6	D2-	USB_HUBP1_ DM	IO, DIFF	USB2 Host Data negative.
7	D2+	USB_HUBP1_DP	IO, DIFF	USB2 Host Data positive
8	GND	USB_GND	Power	Ground

2.5.3 USB 2.0 OTG Interface

The RZ/G1C SBC supports one USB2.0 OTG interface. RZ/G1C CPU's USB0 OTG controller can operate only in Function (Peripheral) mode. The RZ/G1C CPU's USB0 PHY output is directly connected to USB Micro AB Connector(J14). Also, USB over current input from USB Micro AB Connector(J14) is connected to RZ/G1C CPU's USB0_OVC(GP0_1).The Micro AB Connector is physically located on top side of the SBC.

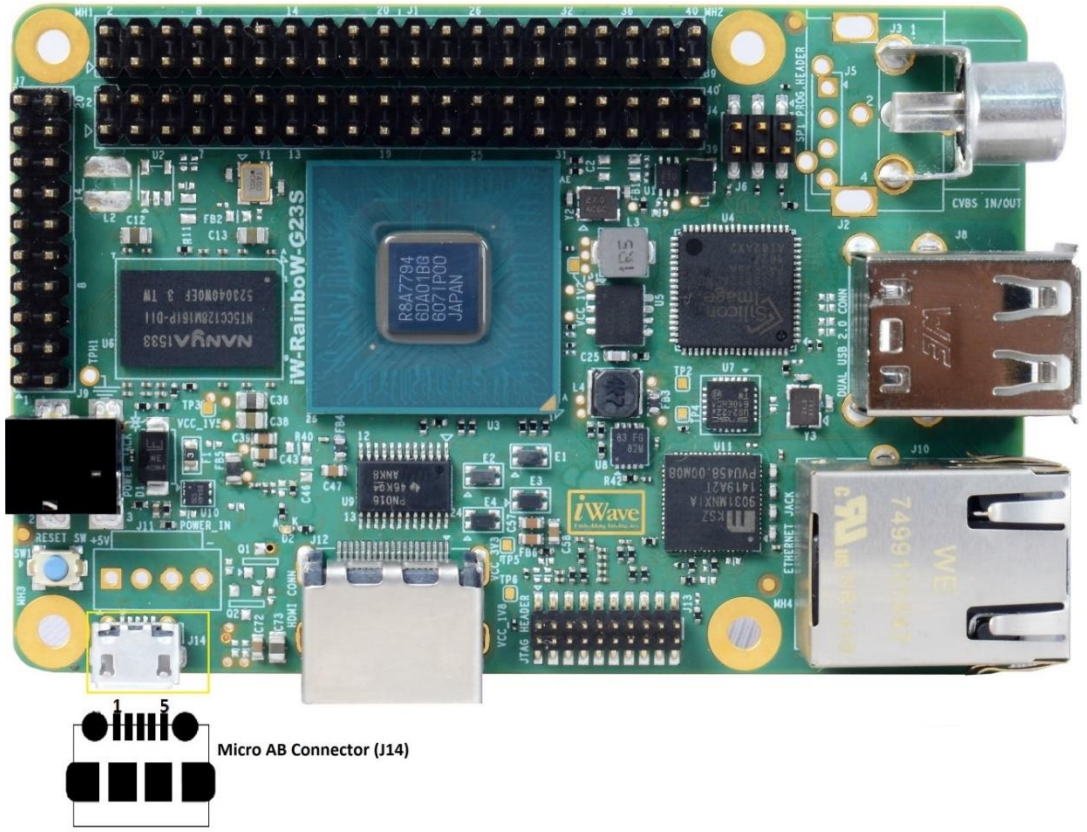

Figure 7: Micro AB Connector

Table 5: USB 2.0 Device Connector Pin Out

Pin No.	Pin Name	Signal Name	Signal Type/ Termination	Description
1	5V	VUSB_5V	Power	5V Supply Voltage
2	D-	USB0_DM	IO, DIFF	USB0 OTG Data negative.
3	D+	USB0_DP	IO, DIFF	USB0 OTG Data positive
4	ID	USB0_OVC (GP0_1)	I, 3.3V CMOS	USB0 Over current sense input.
5	GND	USB_GND	Power	Ground

2.6 Video Features

2.6.1 HDMI Port

The RZ/G1C SBC supports one HDMI output connector to support bigger monitor. The DU0 24bpp RGB signals from RZ/G1C CPU are connected to “SiI9022ACNU” RGB to HDMI Transmitter along with control signals. Also RZ/G1C CPU I2C4 interface is connected to HDMI Transmitter for control & configuration. Output of HDMI transmitter is connected to Standard HDMI connector with ESD protection circuitry. HDMI Output connector (J12) is physically located on top of the board as shown below.

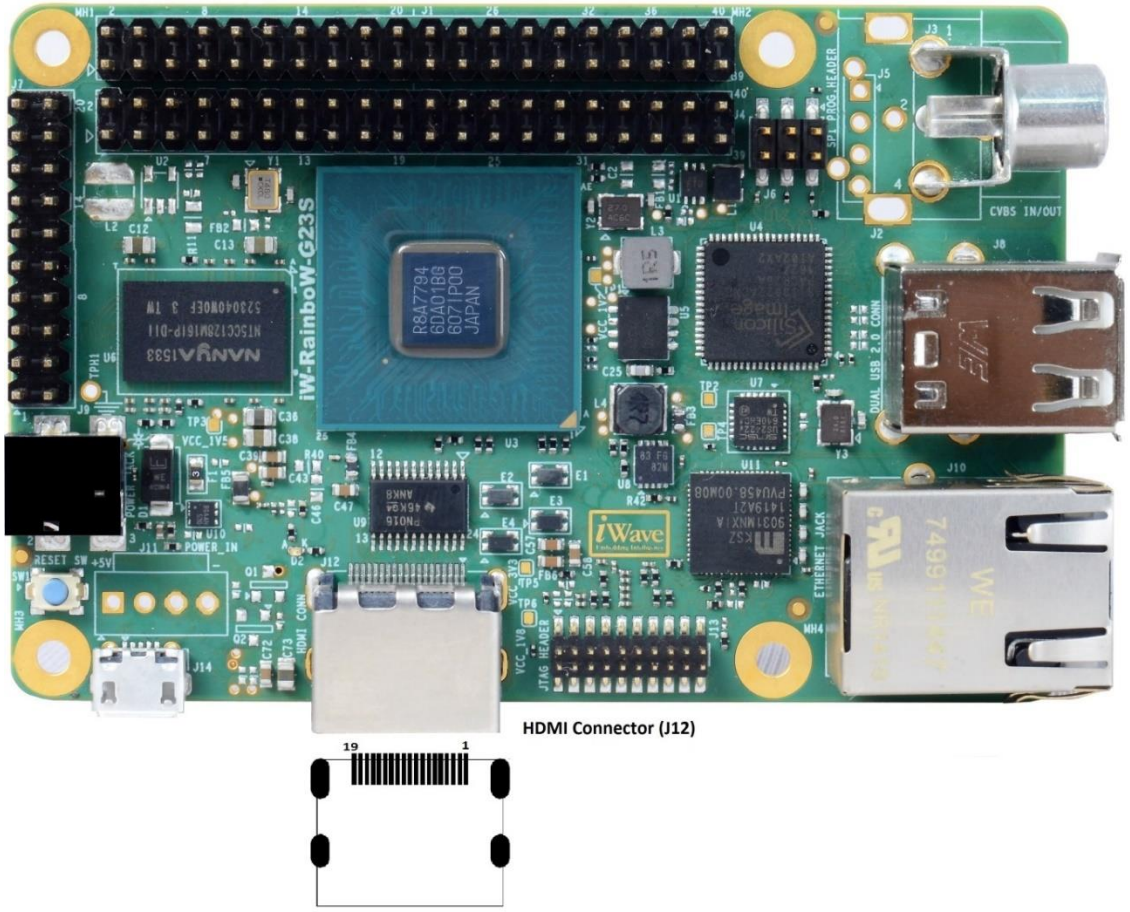

Figure 8: HDMI Connector

Table 6: HDMI Connector Pin Out

Pin No.	Pin Name	Signal Name	Signal Type/ Termination	Description
1	D2+	D2T+	O, TMDS	HDMI data2 pair positive.
2	D2_GND	GND	Power	Ground
3	D2-	D2T	O, TMDS	HDMI data2 pair negative.
4	D1+	D1T+	O, TMDS	HDMI data1 pair positive.
5	D1_GND	GND	Power	Ground

Pin No.	Pin Name	Signal Name	Signal Type/ Termination	Description
6	D1-	D1T	O, TMDS	HDMI data1 pair negative.
7	D0+	D0T+	O, TMDS	HDMI data0 pair positive.
8	D0_GND	GND	Power	Ground
9	D0-	D0T	O, TMDS	HDMI data0 pair negative.
10	CLK+	CLKT+	O, TMDS	Display Clock pair positive.
11	CLK_GND	GND	Power	Ground
12	CLK-	CLKT	O, TMDS	Display Clock pair negative.
13	CEC	CEC	IO, 5V CMOS	Consumer Electronic Control.
14	RSV/NC	NC	-	NC
15	SCL	EM_DDCT_SCL	O, 5V CMOS/ 1.8K PU	EDID I2C Clock.
16	SDA	EM_DDCT_SDA	IO, 5V CMOS 1.8K PU	EDID I2C Data.
17	DDC/CEC_GND	GND	Power	Ground
18	+5V	+5V	O, Power	5V Power Supply.
19	HPD	HPD	I, 5V TTL	HDMI Cable Hot plug detect.

2.6.2 Analog Video IN

The RZ/G1C SBC supports Analog Video In Interface. This “VIN1A” Signal is directly connected from the RCA Jack(J3) to the RZ/G1C CPU. This Analog Video In RCA Jack (J3) is physically located at the top of the board as shown below.

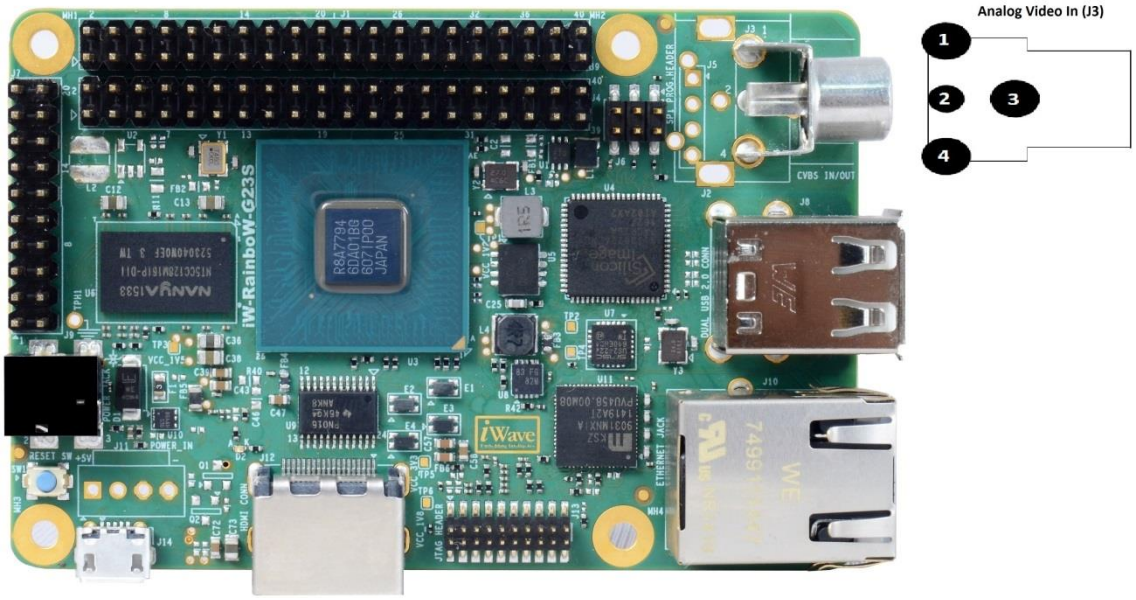

Figure 9: Analog Video IN RCA Jack

Table 7: Analog Video IN RCA Jack Pin Out

Pin No.	Pin Name	Signal Name	Signal Type/ Termination	Description
1	GND	GND	Power	Ground
2	VIDEO	VIDEO	I, Analog	NTSC/PAL composite video input.
3	GND	GND	Power	Ground
4	GND	GND	Power	Ground

2.7 40 Pin Expansion Connector1 Interfaces

The RZ/G1C SBC supports 40 PIN Expansion Connector1, also to pull out more interfaces of RZ/G1C CPU. The interfaces which are available at 40pin Expansion connector1 are explained in the following sections. This iWave 40 PIN Expansion Connector (J1) is physically located at the top of the board as shown below.

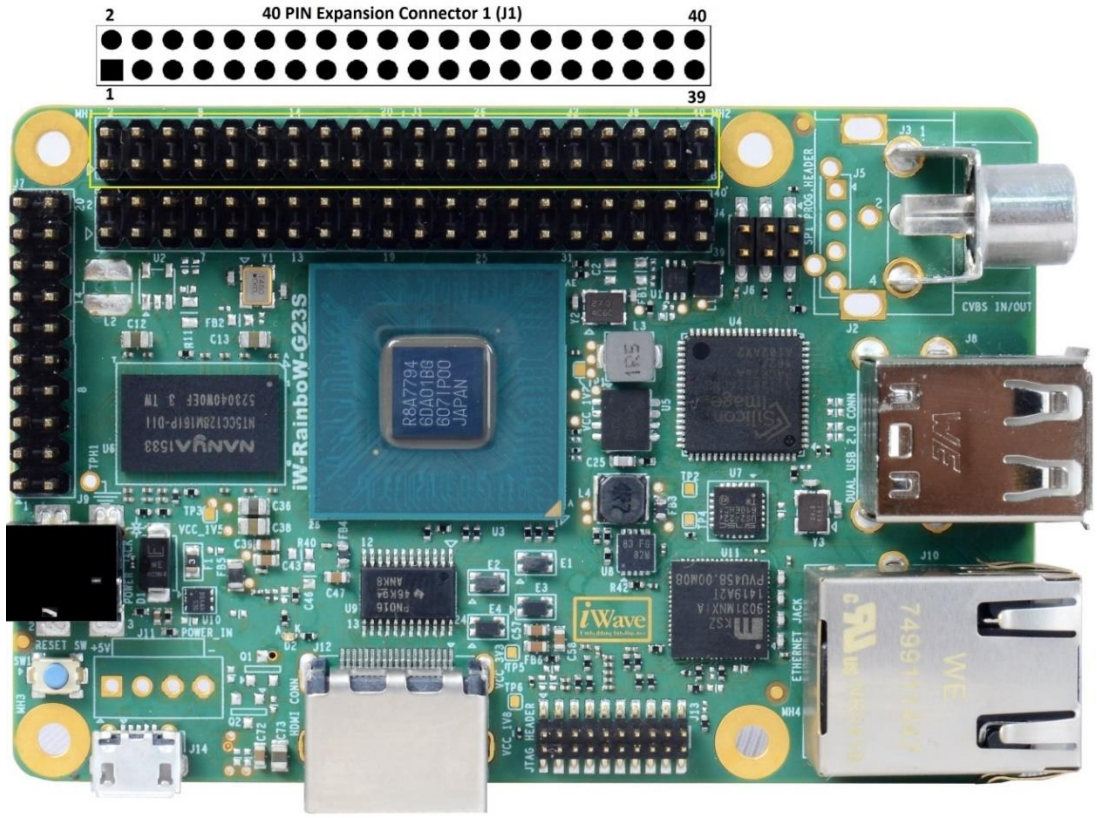

Figure 10: 40 Pin Expansion Connector1

Note: This connector is compatible with Raspberry Pi pinout.

2.7.1 SPI Interface

The RZ/G1C SBC supports one SPI interface. RZ/G1C CPU's MSIOF2 with two chip select is used for SPI interface which supports full-duplex synchronous four-wire serial interface with DMA.

The RZ/G1C CPU's MSIOF controller supports serial formats IIS, SPI (master and slave modes) at max speed of 26Mbps. It supports 32bit x 64 stages for transmit FIFOs & 32bit × 256 stages for receive FIFOs and allows MSB first or LSB first selectable for data transmission and reception.

For more details, refer 40 PIN Expansion connector1 pins 19, 21, 23, 24, 26, 32 pins for MSIOF2 on ***Table 8.***

2.7.2 I2C Interface

The RZ/G1C SBC supports two I2C interface on 40 PIN Expansion connector1. RZ/G1C CPU's I2C4 & I2C1 channels are used for I2C interface which is compatible with the standard NXP I2C bus protocol. It supports standard mode with data transfer rates up to 100kbps and Fast mode with data transfer rates up to 400kbps. It also supports Master/slave functions and Multi-master functions. RZ/G1C CPU is not compliant with the 5V-input.

For more details, refer Expansion Connector 1 pins 3 & 5 for I2C4 and 27 & 28 for I2C1 on ***Table 8.***

2.7.3 GPIO Interface

The RZ/G1C CPU's GPIO blocks provide general-purpose pins that can be configured as either input or output. When configured as an output, it is possible to write to an internal register to control the state driven on the output pin. When configured as an input, it is possible to detect the state of the input by reading the state of an internal register. In addition, the GPIO input can produce interrupt to the CPU core via the interrupt control block when corresponding registers are set.

For more details, refer 40 Pin Expansion Connector 1 Pins 3,7,11,12,15,16,18,22,31,33,35,36,37,40 for GPIO's on ***Table 8.***

2.7.4 Data UART Interface

The RZ/G1C SBC supports 1 Data UART interface on 40 PIN Expansion connector1. RZ/G1C CPU's SCIF2 controller is used for Data UART interface with Transmit & Receive signal on Expansion connector1.

The RZ/G1C CPU's SCIF module has two 16-stage FIFO buffers separately for transmission and reception, which enables fast, efficient, and uninterrupted full duplex communication. It has On-chip baud rate generator that allows any bit rate to be selected. Also it supports DMA transfers.

For more details, refer 40 Expansion connector1 pins 8 & 10 for SCIF2 on ***Table 8.***

2.7.5 PWM6 Interface

The RZ/G1C SBC supports one PWM interface on 40 PIN Expansion Connector1. This PWM timer has a 16-bit timers and supports configurable PWM output cycle within the range from 2 cycles to 224 × 1024 cycles of internal bus clock (i.e. from 30.77 ns to 264 seconds when bus clock = 65 MHz). Also it supports continuous pulse output mode or single pulse output mode which is configurable.

For more details, refer 40 Pin Expansion Connector 1 pins 29 for PWM6 on ***Table 8.***

Table 8: 40 Pin Expansion Connector1 Interfaces

Pin No.	40 Pin Expansion Connector1	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
1	VCC_3V3	NA	O, 3.3V Power	3.3V Power Supply.
2	VCC_5V	NA	O, 5V Power	5V Power Supply.
3	I2C4_SDA(GP5_6)	GP5_6/SDA4_E/ D3/1K PU	IO, 3.3V CMOS	I2C4 Data.
4	VCC_5V	NA	O, 5V Power	5V Power Supply.
5	I2C4_SCL(GP5_7)	GP5_7/SCL4_E/ D2/1K PU	O, 3.3V CMOS	I2C4 Clock.
6	GND	NA	Power	Ground.
7	CLKOUT(GP0_4)	GP0_4/CLKOUT/ AE2	O, 3.3V CMOS	General purpose input/output.
8	SCIF2_TX2_B(GP5_26)	GP5_26/TX2_B/ K2	O,3.3V CMOS	SCIF2 Serial Communication Interface Serial Data Transmitter.
9	GND	NA	Power	Ground.
10	SCIF2_RX2_B(GP5_25)	GP5_25/RX2_B/ K3	I, 3.3V CMOS	SCIF2 Serial Communication Interface Serial Data Receiver.
11	GPIO4/GP4_8	GP4_8/C6	IO, 3.3V CMOS	General purpose input/output.
12	GPIO5/GP4_9	GP4_9/D6	IO, 3.3V CMOS	General purpose input/output.
13	AVB_MAGIC(GP5_15)	GP5_15/AVB_MAGIC/G4	IO, 3.3V CMOS	General purpose input/output.
14	GND	NA	Power	Ground.
15	GPIO14/GP5_21	GP5_21/J4	IO, 3.3V CMOS	General purpose input/output.
16	GP2_26(DU0_DOTCLKOUT 1)	GP2_26/DU0_DOTCLKOUT1/AB 11	O, 3.3V CMOS	General purpose input/output.
17	VCC_3V3	NA	O, 3.3V Power	3.3V Power Supply.
18	GPIO2/GP1_22	GP1_22/AE3	IO, 3.3V CMOS	General purpose input/output.
19	MSIOF2_TXD_A/(GP1_11)	GP1_11/MSIOF2 _TXD_A/Y5	O,3.3V CMOS	SPI Master serial output/Slave serial input (MSIOF2).
20	GND	NA	Power	Ground.
21	MSIOF2_RXD_A(GP1_10)	GP1_10/MSIOF2 _RXD_A/AA1	I,3.3V CMOS	SPI Master serial input/Slave serial output (MSIOF2).
22	GPIO15/GP5_24	GP5_24/J1	IO, 3.3V CMOS	General purpose input/output.
23	MSIOF2_SCK_A(GP1_12	GP1_12/MSIOF2 _SCK_A/Y4	O, 3.3V CMOS	SPI Serial clock (MSIOF2).
24	MSIOF2_SYNC	MSIOF2_SYNC_ A/Y3	O, 3.3V CMOS	SPI frame synchronization signal (MSIOF2).*This signal is used as chip selecet0*
25	GND	NA	Power	Ground.
26	MSIOF2_SS1(GP1_14)	GP1_14/MSIOF2 _SS1/Y2	IO,3.3V CMOS	General purpose input/output.

Pin No.	40 Pin Expansion Connector1	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
27	GPIO7/GP4_23	GP4_23/A4/ 1K PU	IO, 3.3V CMOS	I2C1 Data. *Note: This signal can be configured as GPIO.*
28	GPIO6/GP4_22	GP4_22/B3/ 1K PU	O, 3.3V CMOS	I2C1 Clock. *Note: This signal can be configured as GPIO.*
29	PWM6_C(GP1_4)	GP1_4/PWM6_ C/AB3	O,3.3V CMOS	Pulse Width Modulated Output.
30	GND	NA	Power	Ground.
31	GPIO3/GP4_7	GP4_7/B5	IO, 3.3V CMOS	General purpose input/output.
32	MSIOF2_SS2(GP1_15)	GP1_15/MSIOF2 _SS2/Y1	IO,3.3V CMOS	General purpose input/output.
33	GPIO16/GP5_29	GP5_29/E3	IO, 3.3V CMOS	General purpose input/output.
34	GND	NA	Power	Ground.
35	GPIO9/GP4_25	GP4_25/C4	IO, 3.3V CMOS	General purpose input/output.
36	USB0_PWEN(GP0_0)	GP0_0/USB0_P WEN/Y22	IO, 3.3V CMOS	General purpose input/output.
37	GPIO8/GP4_24	GP4_24/B4	IO, 3.3V CMOS	General purpose input/output.
38	QSPI0_IO3(GP1_20)	GP1_20/QSPI0_I O3/AC5	IO, 3.3V CMOS	General purpose input/output. *Note: This signal is shared with SPI Flash Reset pin through resistor and default not populated*
39	GND	NA	Power	Ground.
40	GPIO10/GP5_0	GP5_0/A3	IO, 3.3V CMOS	General purpose input/output.

2.8 40 Pin Expansion Connector2 Interfaces

The RZ/G1C SBC supports 40 PIN Expansion Connector2, also to pull out more interfaces of RZ/G1C CPU. The interfaces which are available at 40pin Expansion connector2 are explained in the following sections. This iWave 40 PIN Expansion Connector (J4) is physically located at the top of the board as shown below.

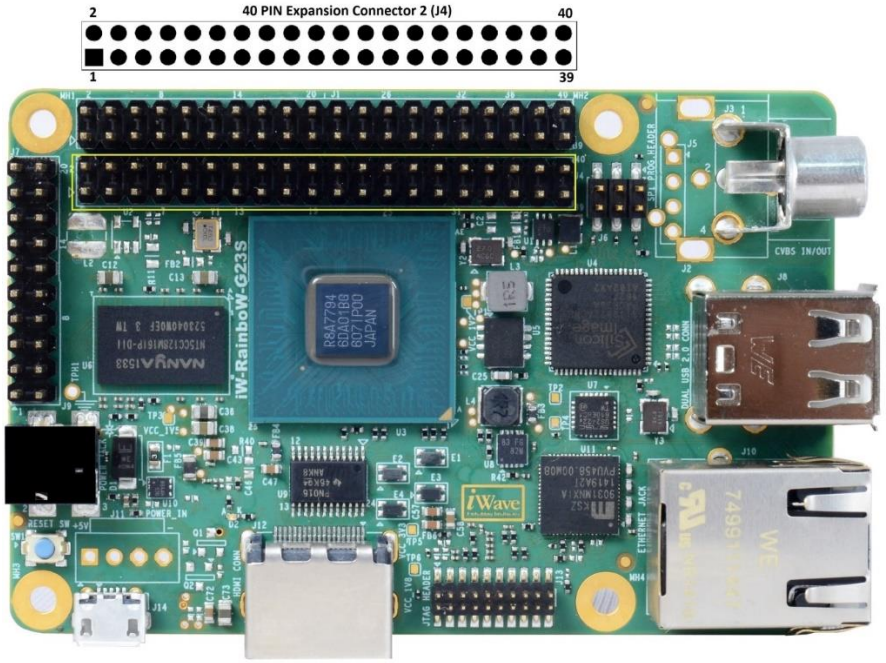

Figure 11: 40 Pin Expansion Connector2

2.8.1 LVDS Interface

The RZ/G1C SBC supports one LVDS interface on 40 PIN Expansion Conenctor2. Five pairs of differential output conforming to the TIA/EIA-644 standard (four pairs for data and one pair for the clock). LVDS interface supports maximum dot clock frequency of 13.4 to 87MHz.

For more details, refer Expansion connector2 pin 7, 9, 13, 15, 19, 21, 25, 27, 31 & 33 on ***Table 9.***

2.8.2 CAN Interface

The RZ/G1C SBC supports one CAN interface on 40 PIN Expansion connector2. RZ/G1C CPU's CAN module supports two channels in which CAN0 channel is connected to Expansion connector2.

The RZ/G1C CPU's CAN module complies with the ISO11898-1 Specifications and supports programmable bit rate up to 1 Mbps with both formats of messages namely the standard identifier (11 bits) and extended ID (29 bits).It also supports 64 mailboxes in two selectable mailbox mode Normal mailbox mode and FIFO mailbox mode. To connect external CAN module to this bus, it is necessary to add transceiver in between.

For more details, refer Expansion connector2 pins 16 & 18 on ***Table 9.***

2.8.3 I2S Audio Interface

The RZ/G1C Supports three I2S audio interface port on 40 PIN Expansion connector2. RZ/G1C CPU's SSI0, SSI1 and SS9 of SSIU is used for I2S interface.

The RZ/G1C CPU's serial sound interface (SSI) is a transceiver module designed to send or receive audio data interfacing with a variety of devices offering I2S format. It also supports master/slave functions and multi-channel format functions. The frequency range of SCK signal is from 297.3 kHz to 12.5MHz at master mode and from 297.3 kHz to 15.1 MHz at slave mode. SSI Module supports TDM format operation at 44.1- or 48-kHz sampling rate.

For more details, refer Expansion connector2 pins 1, 3, 5, 6, 8, 10 & 12 on ***Table 9.***

2.8.4 Data UART Interface

The RZ/G1C SBC supports 3 Data UART interface on 40 PIN Expansion connector2. RZ/G1C CPU's SCIF5 controller is used for Data UART interface with Transmit & Receive signal on Expansion connector2. RZ/G1C CPU's HSCIF1 and HSCIF2 controller is used for Data UART interface with hardware flow control for request to send and clear to send signals on Expansion connector2.

The RZ/G1C CPU's SCIF module has two 16-stage FIFO buffers separately for transmission and reception, which enables fast, efficient, and uninterrupted full duplex communication. It has On-chip baud rate generator that allows any bit rate to be selected. Also it supports DMA transfers.

The RZ/G1C CPU's HSCIF1 and HSCIF2 is a high speed serial communication interface with built-in FIFO buffers that handles asynchronous communication. It has two 128-stageFIFO buffers separately for transmission and reception, which enables fast, efficient, and uninterrupted communication.

For more details, refer Expansion connector2 pins 18, 20, 22, 24 and 26 for HSCIF2, 28 & 30 for SCIF5, and 32, 34, 36, 38 HSCIF1 on ***Table 9.***

2.8.5 I2C Interface

The RZ/G1C SBC supports one I2C interface on 40 PIN Expansion connector2. RZ/G1C CPU's I2C3 channel is used for I2C interface which is compatible with the standard NXP I2C bus protocol. It supports standard mode with data transfer rates up to 100kbps and Fast mode with data transfer rates up to 400kbps. It also supports Master/slave functions and Multi-master functions. RZ/G1C CPU is not compliant with the 5V-input.

For more details, refer Expansion connector2 pin 37 & 39 for I2C3 on ***Table 9.***

2.8.6 PWM Interface

The RZ/G1C SBC supports one PWM interface on iWave 40 PIN Expansion Connector2. RZ/G1C CPU's PWM0 channel is used for PWM interface. This PWM timer has a 10-bit counter and supports configurable PWM output cycle within the range from 2 cycles to 224 × 1024 cycles of internal bus clock (i.e. from 30.77 ns to 264 seconds when bus clock = 65 MHz). Also it supports continuous pulse output mode or single pulse output mode.

For more details, refer Expansion connector2 pin 40 on ***Table 9.***

Table 9: 40 Pin Expansion Connector2 Interfaces

Pin No.	40 Pin Expansion Connector2	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
1	SSI_SCK1_C(GP0_5)	GP0_5/SSI_SCK 1_C/A13	O, 3.3V CMOS	Audio Serial clock for SSI channel 1.
2	VCC_3V3	NA	O, 3.3V Power	3.3V Power Supply. *Note: V_LED_K power supply can be provided from LVDS Regulator. By default through resistor and default not populated.*
3	SSI_SDATA1_C(GP0_7)	GP0_7/SSI_SDA TA1_C/B13	IO, 3.3V CMOS	Audio Serial data for SSI channel 1.
4	VCC_5V	NA	O, 5V Power	5V Power Supply. *Note: V_LED_A power supply can be provided from LVDS Regulator. By default through resistor and default not populated..*
5	SSI_WS1_C(GP0_6)	GP0_6/SSI_WS1 _C/D13	IO, 3.3V CMOS	Audio Word select for SSI channel 1.
6	SSI_SCK0129_B(GP0_8)	GP0_8/SSI_SCK 0129_B/D14	IO, 3.3V CMOS	Audio Serial clock for SSI channel 0.
7	TXOUT3P	TXOUT3P/AD17	O, 3.3V LVDS	LVDS channel differential pair 3 positive.
8	SSI_SDATA0_B(GP0_10)	GP0_10/SSI_SD ATA0_B/B14	IO, 3.3V CMOS	Audio Serial data for SSI channel 0.
9	TXOUT3M	TXOUT3M/AE1 7	O, 3.3V LVDS	LVDS channel differential pair 3 negative.
10	SSI_WS0129_B(GP0_9)	GP0_9/SSI_WS0 129_B/C14	IO, 3.3V CMOS	Audio Word select for SSI channel 0.
11	GND	NA	Power	Ground.
12	SSI_SDATA9_B(GP4_21)	GP4_21/SSI_SD ATA9_B/D18	IO, 3.3V CMOS	Audio Serial data for SSI channel 9.
13	TXCLKOUTP	TXCLKOUTP/AB 16	O, 3.3V LVDS	LVDS channel differential clock positive.

Pin No.	40 Pin Expansion Connector2	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
14	CAN0_RX_A(GP0_11)	GP0_11/CAN0_RX_A/A8	I, 3.3V CMOS	Receive input for CAN bus.
15	TXCLKOUTM	TXCLKOUTM/AC16	O, 3.3V LVDS	LVDS channel differential clock positive.
16	CAN0_TX_A(GP0_12)	GP0_12/CAN0_TX_A/B8	O, 3.3V CMOS	Transmit output for CAN bus.
17	GND	NA	Power	Ground.
18	HSCIF2_HCTS2(GP1_8)	GP1_8/HCTS2#/AA3	I, 3.3V CMOS	High Speed Serial Communication Interface (HSCIF2) Clear to Send.
19	TXOUT2P	TXOUT2P/AD15	O, 3.3V LVDS	LVDS channel differential pair 2 positive.
20	HSCIF2_HRTS2(GP1_9)	GP1_9/HRTS2#/AA2	O, 3.3V CMOS	High Speed Serial Communication Interface (HSCIF2) Ready to Send.
21	TXOUT2M	TXOUT2M/AE15	O, 3.3V LVDS	LVDS channel differential pair 2 negative.
22	HSCIF2_HRX2(GP1_5)	GP1_5/HRX2/AB2	I, 3.3V CMOS	High Speed Serial Communication Interface (HSCIF2) Serial Data Receiver.
23	GND	NA	Power	Ground.
24	HSCIF2_HTX2(GP1_6)	GP1_6/HTX2/AB1	O, 3.3V CMOS	High Speed Serial Communication Interface (HSCIF2) Serial Data Transmitter.
25	TXOUT1P	TXOUT1P/AB14	O, 3.3V LVDS	LVDS channel differential pair 1 positive.
26	HSCIF2_HSCK2(GP1_7)	GP1_7/HSCK2/AA4	IO, 3.3V CMOS	High Speed Serial Communication Interface (HSCIF2) clock
27	TXOUT1M	TXOUT1M/AC14	O, 3.3V LVDS	LVDS channel differential pair 1 negative.
28	SCIF5_RX5_B(GP1_0)	GP1_0/RX5_B/AD2	I, 3.3V CMOS	Serial Communication Interface (SCIF5) Serial Data Receiver.
29	GND	NA	Power	Ground.
30	SCIF5_TX5_B(GP1_1)	GP1_1/TX5_B/AD1	O, 3.3V CMOS	Serial Communication Interface (SCIF5) Serial Data Transmitter.
31	TXOUT0P	TXOUT0P/AD13	O, 3.3V LVDS	LVDS channel differential pair 0 positive.
32	HSCIF1_HCTS1_A(GP4_12)	GP4_12/HCTS1#_A/E8	I, 3.3V CMOS	High Speed Serial Communication Interface (HSCIF1) Clear to Send.
33	TXOUT0M	TXOUT0M/AE13	O, 3.3V LVDS	LVDS channel differential pair 0 negative.
34	HSCIF1_HRTS1_A(GP4_13)	GP4_13/HRTS1#_A/D7	O, 3.3V CMOS	High Speed Serial Communication Interface (HSCIF1) Ready to Send.

Pin No.	40 Pin Expansion Connector2	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
35	PRESETOUT#	PRESETOUT#/AC20	O, 3.3V CMOS	Reset Output. *PRESETOUT# is connected to this pin through resistor and default populated.* *Note: Main Reset signal is shared with QSPI0_IO2(GP1_19).By default through resistor and default not populated.*
36	HSCIF1_HTX1_A(GP4_11)	GP4_11/HTX1_A/B7	O, 3.3V CMOS	High Speed Serial Communication Interface (HSCIF1) Serial Data Transmitter.
37	I2C3_SCL(GP5_1)	GP5_1/SCL3_C/A2/1K PU	O, 3.3V CMOS	I2C3 Clock.
38	HSCIF1_HRX1_A(GP4_10)	GP4_10/HRX1_A/A7	I, 3.3V CMOS	High Speed Serial Communication Interface (HSCIF1) Serial Data Receiver.
39	I2C3_SDA(GP5_2)	GP5_2/SDA3_C/B2/1K PU	IO, 3.3V CMOS	I2C3 Data.
40	PWM0_C(GP5_11)	GP5_11/PWM0_C/H4	O,3.3V CMOS	Pulse Width Modulated Output.

2.9 20 Pin Expansion Connector Interfaces

The RZ/G1C SBC supports 20 PIN Expansion Connector also to pull out more interfaces of RZ/G1C CPU. The interfaces which are available at 20pin Expansion connector are explained in the following sections. This iWave 20 PIN Expansion Connector (J7) is physically located at the top of the board as shown below.

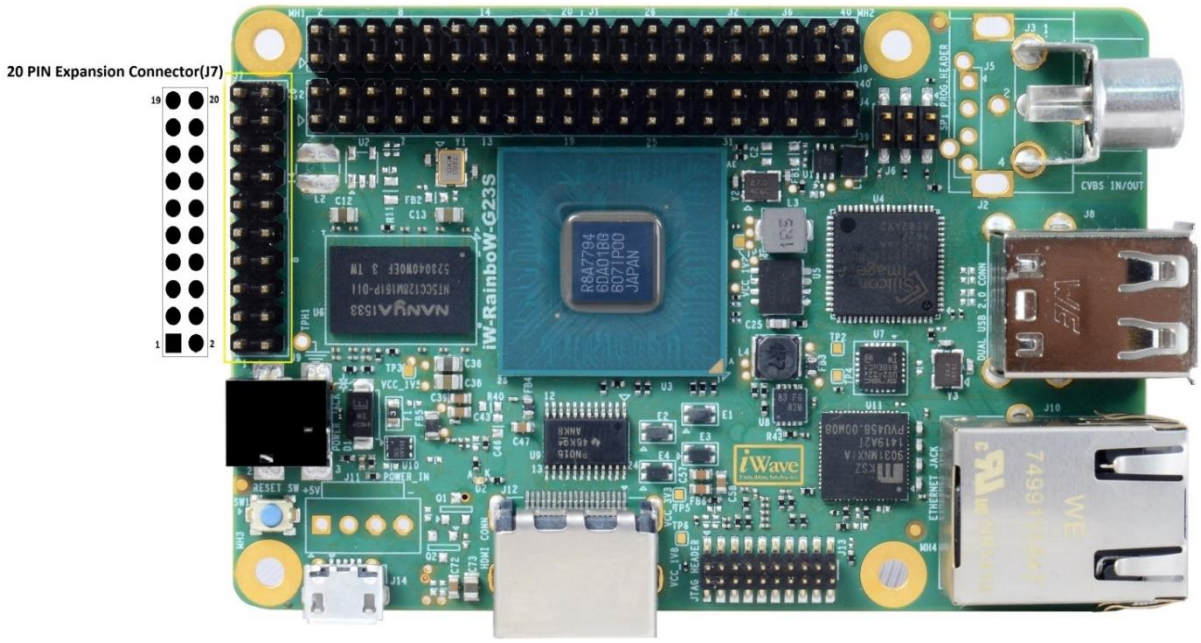

Figure 12: 20 Pin Expansion Connector

2.9.1 Parallel Camera Interface

The RZ/G1C SBC supports one parallel camera interface. RZ/G1C CPU VIN0 channel is used for this 8bit parallel camera interface. Also Camera interface is directly connected to 20 PIN Expansion Connector.

The RZ/G1C CPU's Video Input Module (VIN0) is a video capture module that supports YCbCr-422 data through the ITU-R BT.601, ITU-R BT.656 or ITU-R BT.709 interface and RGB data through the ITUR BT.601 or ITU-R BT.709 interface. The VIN0 supports Vertical and Horizontal Scaling where the image can be scaled up and down up to three times in the vertical and two times in the horizontal directions. Also, it has two clipping circuits, which independently handle images with up to 2048 × 2048 pixels. The VIN provides a colour space conversion function from YCbCr-422 to RGB, a format conversion function from RGB to ARGB.

For more details, refer 20 PIN Expansion connector pins for Parallel Camera 1,3,9,11,13,2,4,8,10,12,14,16 ***Table 10***

2.9.2 UART Interface

The RZ/G1C SBC supports Two UART interfaces on 20 PIN Expansion connector in which one is for Debug UART interface and other one for DATA UART interface. RZ/G1C CPU's SCIF1 controller is used for Debug UART and SCIF4 controller is used for Data UART interface.

The RZ/G1C CPU's SCIF module has two 16-stage FIFO buffers separately for transmission and reception, which enables fast, efficient, and uninterrupted full duplex communication. It has On-chip baud rate generator that allows any bit rate to be selected. Also it supports DMA transfers.

For more details, 20 PIN Expansion connector pins 18 & 20 for SCIF4, 17 & 19 for SCIF1, on ***Table 10.***

2.9.3 PWM2 Interface

The RZ/G1C SBC supports one PWM interface on 20 PIN Expansion Connector. This PWM timer has a 16-bit timers and supports configurable PWM output cycle within the range from 2 cycles to 224 × 1024 cycles of internal bus clock (i.e. from 30.77 ns to 264 seconds when bus clock = 65 MHz). Also it supports continuous pulse output mode or single pulse output mode which is configurable.

For more details, 20 PIN Expansion connector pins for PWM 2 on ***Table 10***

Table 10: 20 PIN Expansion Connector Interfaces

Pin No.	iWave 20 PIN Expansion Connector	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
1	VI0_CLK/AVB_COL/ (GP5_18)	GP5_18/AVB_COL/VI0_CLK/H2	I, 3.3V CMOS	Video Input Channel0 pixel clock. *Note: This signal is optionally connected to Ethernet PHY AVB COL Pin through resistor and default not populated.*
2	VI0_HSYNC(GP5_30)	GP5_30/VI0_HSYNC#/E4	I, 3.3V CMOS	Video Input Channel0 Horizontal synchronization signal.
3	VI0_VSYNC(GP5_31)	GP5_31/VI0_VSYNC#/E1	I, 3.3V CMOS	Video Input Channel0 Vertical synchronization signal.
4	VI0_CLKENB(GP5_28)	GP5_28/VI0_CLKENB/E2	I, 3.3V CMOS	Video Input Channel0 data enable signal.
5	GND	GND	Power	Ground.
6	VCC	VCC_5V	O, 5V Power	5V Power Supply.
7	PWM2_D(GP5_27)_EXP	GP5_27/PWM2_D/K1	O, 3.3V CMOS	Pulse Width Modulated Output.
8	VI0_G2(GP4_4)	GP4_4/VI0_G2/A6	I, 3.3V CMOS	Video Input0 Data 2.
9	VI0_G4(GP4_6)	GP4_6/VI0_G4/A5	I, 3.3V CMOS	Video Input0 Data 4.
10	VI0_G3(GP4_5)	GP4_5/VI0_G3/B6	I, 3.3V CMOS	Video Input0 Data 3.
11	VI0_G7(GP5_10)	GP5_10/VI0_G7/G1	I, 3.3V CMOS	Video Input0 Data 7.
12	VI0_G0(GP4_2)	GP4_2/VI0_G0/C5	I, 3.3V CMOS	Video Input0 Data 0.
13	VI0_G1(GP4_3)	GP4_3/VI0_G1/D5	I, 3.3V CMOS	Video Input0 Data 1.
14	VI0_G5(GP5_8)	GP5_8/VI0_G5/F5	I, 3.3V CMOS	Video Input0 Data 5.
15	GND	GND	Power	Ground.
16	VI0_G6(GP5_9)	GP5_9/VI0_G6/G2	I, 3.3V CMOS	Video Input0 Data 6.
17	SCIF1_RX1_B(GP5_19)	GP5_19/RX1_B/F4	I, 3.3V CMOS	SCIF1 Serial data receiver for debug.
18	SCIF4_RX4_B(GP1_2)	GP1_2/RX4_B/AC2	I, 3.3V CMOS	SCIF4 Serial data receiver input.
19	SCIF1_TX1_B(GP5_20)	GP5_20/TX1_B/H1	O, 3.3V CMOS	SCIF1 Serial data transmitter for debug.
20	SCIF4_TX4_B(GP1_3)	GP1_3/TX4_B/AC1	O, 3.3V CMOS	SCIF4 Serial data transmitter output.

2.10 Other Features

2.10.1JTAG Header

The RZ/G1C SBC supports JTAG Interface for CPU Debug purpose. This provides debug and test control with the maximum security. This is connected to JTAG controller of the RZ/G1C CPU and operates at 1.8 Voltage level .This Signals are directly connected from JTAG connector to RZ/G1C CPU. This JTAG Connector (J13) is physically located at the top of the board as shown below.

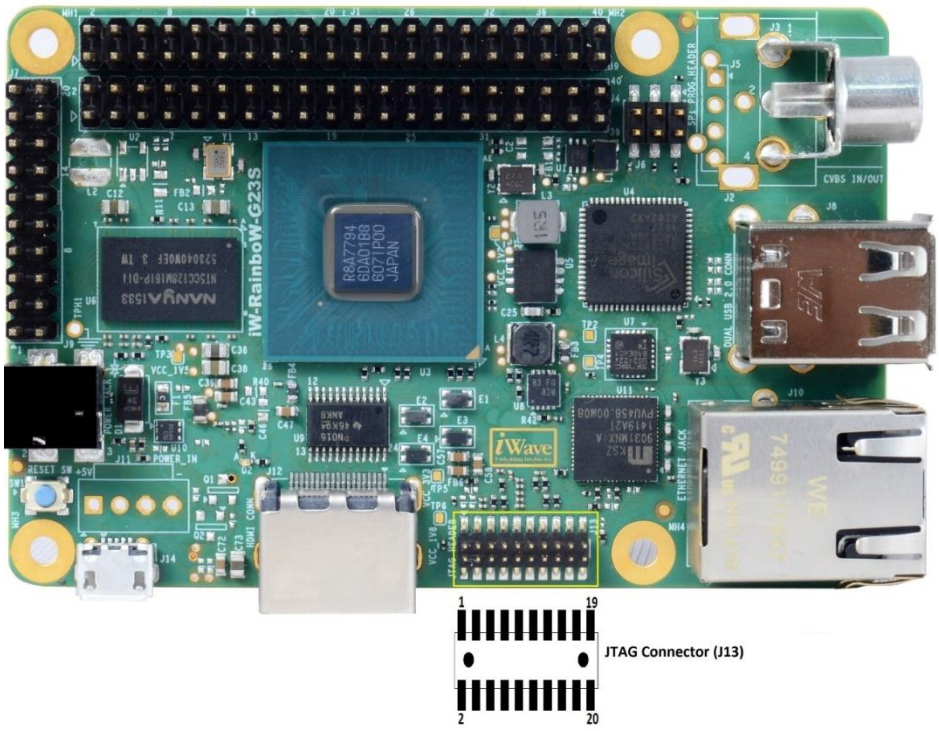

Figure 13: JTAG Connector

Table 11: JTAG Connector Pin Out

Pin No.	Pin Name	Signal Name	Signal Type/ Termination	Description
1	VCC	VCC_1V8	O, 1.8V Power	VREF reference Voltage.
2	VCC	VCC_1V8	O, 1.8V Power	Supply Voltage.
3	JTAG_TRSTB	JTAG_TRSTB	I, 1.8V CMOS/ 10K PD	JTAG test reset signal.
4	GND	GND	Power	Ground.
5	JTAG_TDI	JTAG_TDI	I, 1.8V CMOS/ 10K PU	JTAG test data Input.
6	GND	GND	Power	Ground.
7	JTAG_TMS	JTAG_TMS	I, 1.8V CMOS/ 10K PU	JTAG test mode select.
8	GND	GND	Power	Ground.

Pin No.	Pin Name	Signal Name	Signal Type/ Termination	Description
9	JTAG_TCK	JTAG_TCK	I, 1.8V CMOS/ 10K PU	JTAG test clock.
10	GND	GND	Power	Ground.
11	-	-	-	NC
12	GND	GND	Power	Ground.
13	JTAG_TDO	JTAG_TDO	I, 1.8V CMOS	JTAG test data Output.
14	GND	GND	Power	Ground.
15	RSTBN	RSTBN	I, 1.8V CMOS/ 10K PU	Reset Signal.
16	GND	GND	Power	Ground.
17	NC	NC	10K PD	NC
18	GND	GND	Power	Ground.
19	-	-	10K PD	NC
20	GND	GND	Power	Ground.

2.10.2 Reset Switch

The RZ/G1C SBC supports Push button switch (SW1) to reset the RZ/G1C CPU. “RST_BTN” signal is directly connected from Reset Push button switch. This Reset Push button switch (SW1) is physically located at the top of the board as shown below.

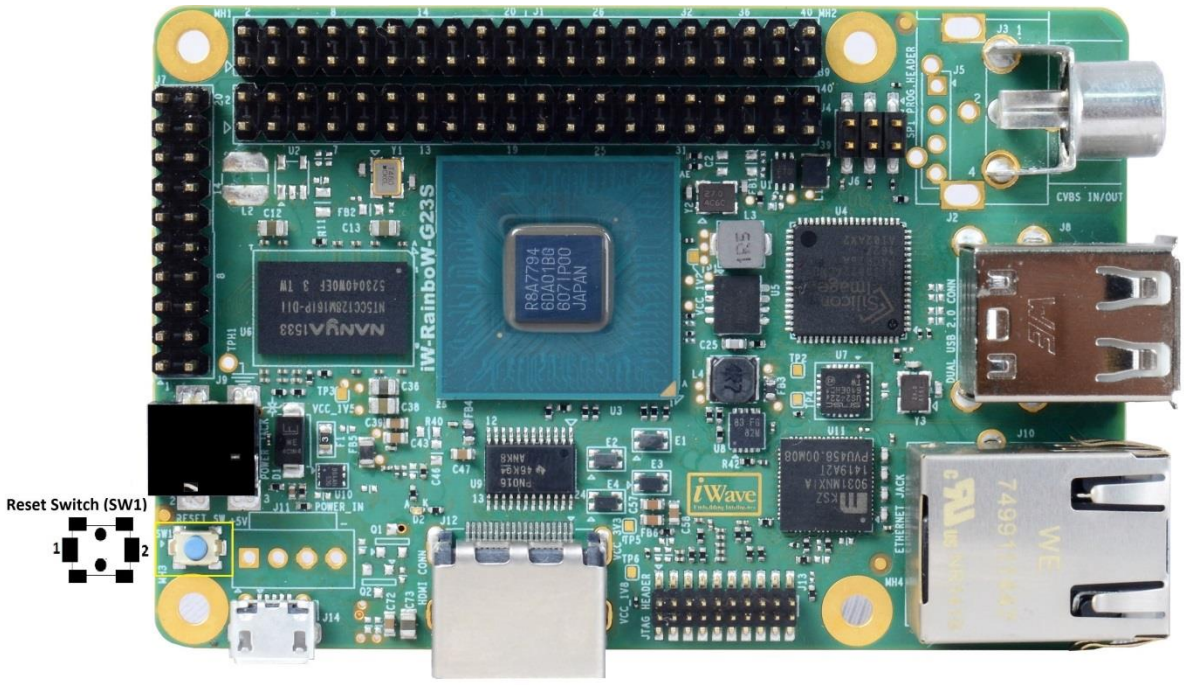

Figure 14: Reset Switch

3. TECHNICAL SPECIFICATION

This section provides detailed information about the RZ/G1C SBC technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Electrical Characteristics

3.1.1 Power IN Connector

The RZ/G1C SBC is designed to work with a +5V external power and uses on board voltage regulator for internal power management. 5V power input from an external power supply is connected to the SBC through Power Jack (J9). This 1.65mm x 4.40mm barrel connector Jack should fit standard DC Plugs with an inner dimension of 1.7mm and an outer dimension of 4mm.This Power Jack (J9) is physically located at the top of the board as shown below.

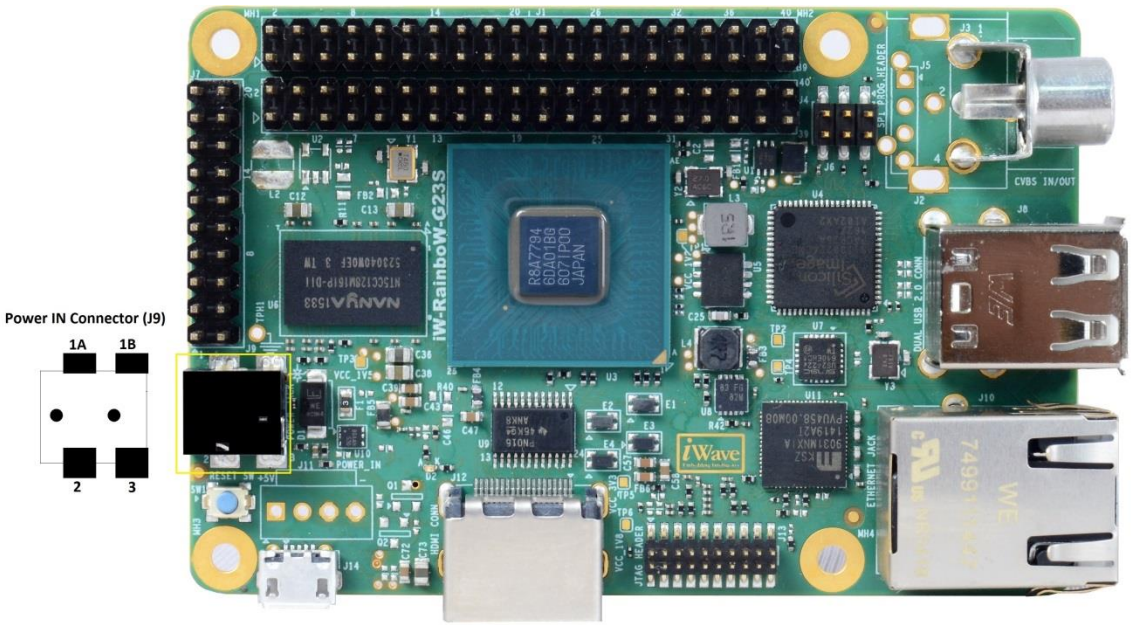

Figure 15: Power IN Connector

Table 12: Power IN Connector Pin Out

Pin No.	Pin Name	Signal Name	Signal Type/ Termination	Description
1	VCC(A & B)	Power IN	5V, Power	Input Supply Voltage.
2	GND	GND	Power	Ground.
3	GND	GND	Power	Ground.

3.1.2 Power Input Requirement

The below table provides the Power Input Requirement of RZ/G1C SBC.

Table 13: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC_5V[1]	4.75V	5V	5.25V	±50mV

[1] RZ/G1C SBC is designed to work with VCC_5V input power rail from Power connector.

Table 14: Power Consumption[1]

Task/Status	Power Rail	Current Drawn/Power Consumption
Run Mode Power Consumption		
TBD	TBD	TBD
Low Power Mode Power Consumption		
TBD	TBD	TBD

[1] Power consumption measurements have been done in iWave's RZ/G1C CPU based SBC (TBD).

3.2 EnvironmentalCharacteristics

3.2.1 Environmental Specification

The below table provides the Environment specification of RZ/G1C SBC.

Table 15: Environmental Specification

Parameters	Min	Max
Operating temperature range[1,2]	-40°C	85°C
Humidity - Operating	10%RH	90%RH

[1] iWave guarantees the component selection for the given operating temperature. The operating temperature at the system level will be affected by the various system components like system enclosure, air circulation in the system, system power supply etc. Based on the system design, specific heat dissipating approach might be required from system to system. It is recommended to do the necessary system level thermal simulation and find necessary thermal solution in the system before using this board in the end application.

[2] If Micro SD connector is supported in RZ/G1C SBC, then operating temperature range is -25°C to 85°C.

3.2.2 RoHS Compliance

iWave's RZ/G1C SBC is designed by using RoHS compliant components and manufactured on lead free production process.

3.2.3 Electrostatic Discharge

iWave's RZ/G1C SBC is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use the SBC except at an electrostatic free workstation.

3.3 MechanicalCharacteristics

3.3.1 RZ/G1C SBC Mechanical Dimensions

RZ/G1C SBC PCB size is 85mm x 56mm x 1.6mm. SBC mechanical dimension is shown below.

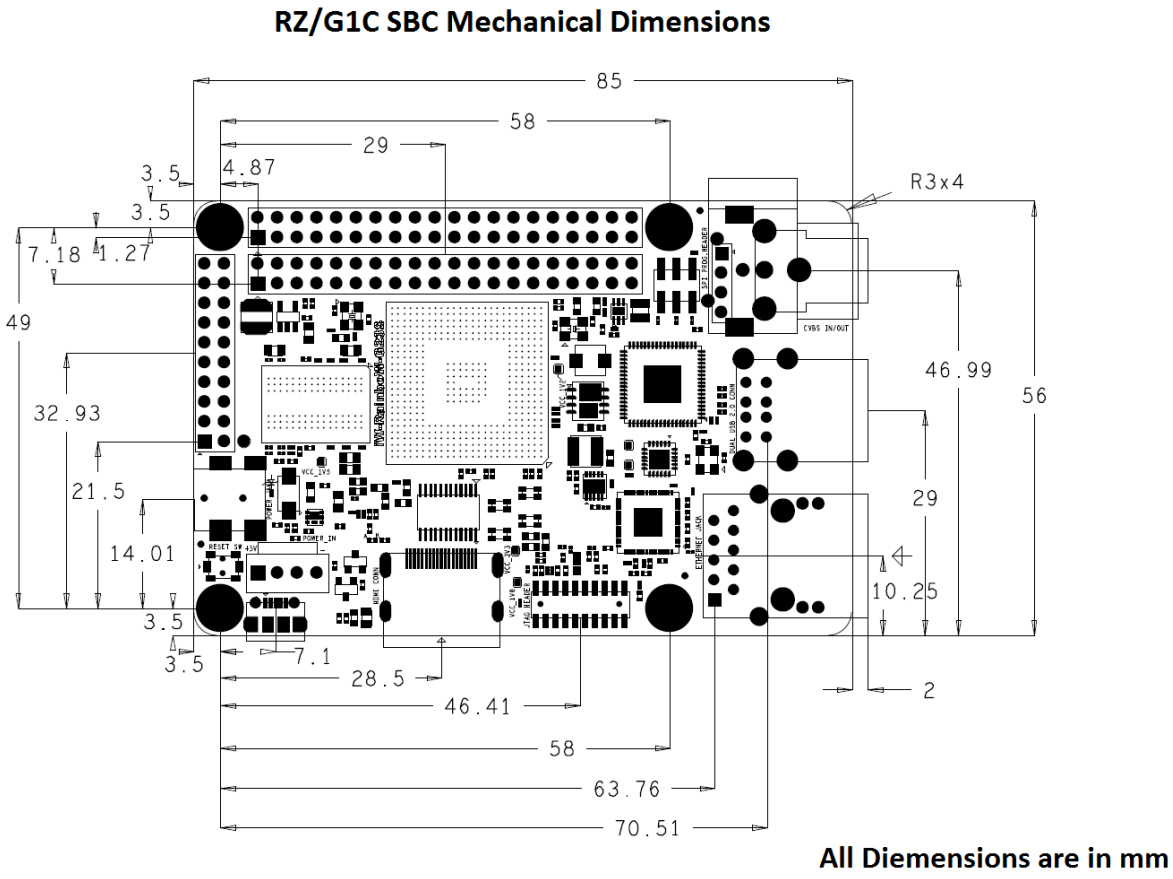

Figure 16: Mechanical dimension of RZ/G1C SBC - Top View

RZ/G1C SBC PCB thickness is 1.6mm±0.1mm, top side maximum height connector is Dual USB Stack connector (15.97mm) followed by Ethernet connector (14.37mm) and bottom side maximum height component is Inductor (4.50mm) followed by Bulk Capacitor (2.5mm). Please refer the below figure which gives height details of the RZ/G1C SBC.

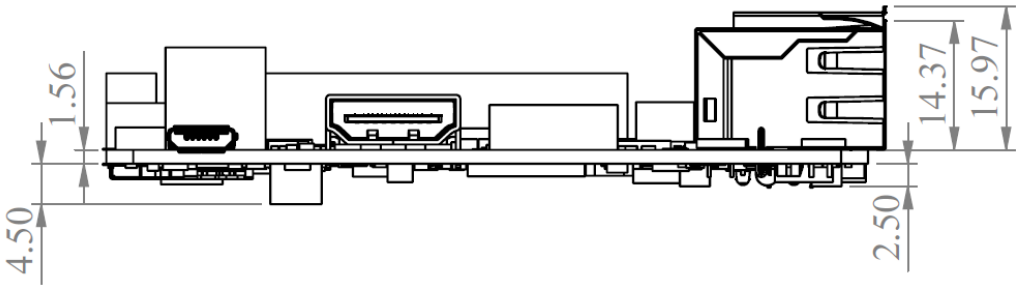

Figure 17: Mechanical dimension of RZ/G1C SBC- Side View

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for different RZ/G1C SBC variations. Please contact iWave for orderable part number of higher RAM memory size or Flash memory size SBC configurations. Also if the desired part number is not listed in below table or if any custom configuration part number is required, please contact iWave.

Table 16: Orderable Product Part Numbers

Product Part Number	Description	Temperature
RZ/G1C SBC - 512MB RAM & 4GB eMMC Flash		
		Industrial

Important Note: Some of the above-mentioned Part Number is subject to MOQ purchase. Please contact iWave for further details.

Note: For SBC identification purpose, Product Part Number and SBC Unique Serial Number are pasted as Label with Barcode readable format on SBC.


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